EVALUATION OF CARRIER BASED NEUTRAL POINT POTENTIAL REGULATOR WITH SMALL DC LINK CAPACITORS FOR DIODE CLAMPED INVERTER

***N.Susheela,**P.Satish Kumar,**

**Department of Electrical Engineering,*
University College of Engineering (A),Osmania University,
Hyderabad, Telangana
***Department of Electrical Engineering,*
University College of Engineering (A),Osmania University,
Hyderabad, Telangana

ABSTRACT

This paper presents the diode clamped inverter fed induction motor drives with DC-link voltage stabilisation and small DC-link capacitors. The diode bridge rectifier is used as a front end converter. The small DC-link capacitors have an advantage of low input line current total harmonic distortion (THD) as compared to the THD in case of the large DC-link capacitors. As well as DC-link unbalance may overstress the capacitors and devices during a sudden regenerative load increases and it can also cause problems due to over voltage and under voltage trips. For neutral–point voltage to be stable the inverter requires zero average neutral-point current. The carrier-based technique that allows modelling of the neutral-point voltage dynamics as a continuous function of power drawn from the inverter is implemented. An implementation of the controller using 7.5kW induction motor is carried out with dc-link capacitors of 3.3mF and 14 µF. The model shows that the neutral-point current is proportional to the power drawn from the inverter, and it enables the use of classical control theory for the design of neutral-point voltage controller. A simple proportional integral controller is designed for the neutral-point voltage control on the basis of the continuous model. The phase disposition carrier based modulation strategy is used for implementation of three level diode clamped inverter using MATLAB/Simulink.

Keywords: *diode clamped inverter; multilevel inverter; pulse width modulation; neutral point voltage-control;*

INTRODUCTION

Variable frequency drives has increasing rapidly in the present trend utilization due to the advantages possessed by multilevel inverters. The diode clamped multilevel inverter which is also called as neutral point clamped (NPC) multilevel inverter is being used for high and medium voltage drives. This topology is also used for low voltage applications [1-4]. Due to the variation of Neutral point voltage, large capacitors are required which introduces high input line current total harmonic distortion (THD)[5-6]. This paper presents to replace the high DC link capacitors with low DC link capacitors. The small dc-link capacitors may not maintain capacitor voltage balance, even with zero

neutral-point current. This may happen due to nonlinearities present in the circuit. This requires a fast control of the neutral-point voltage. The design method for optimum performance is discussed. The implementation of the proposed modulation strategy and the controller is very simple.

Fig. 1 shows the very popular topological structure of 3-phase, 3-level diode clamped inverter.

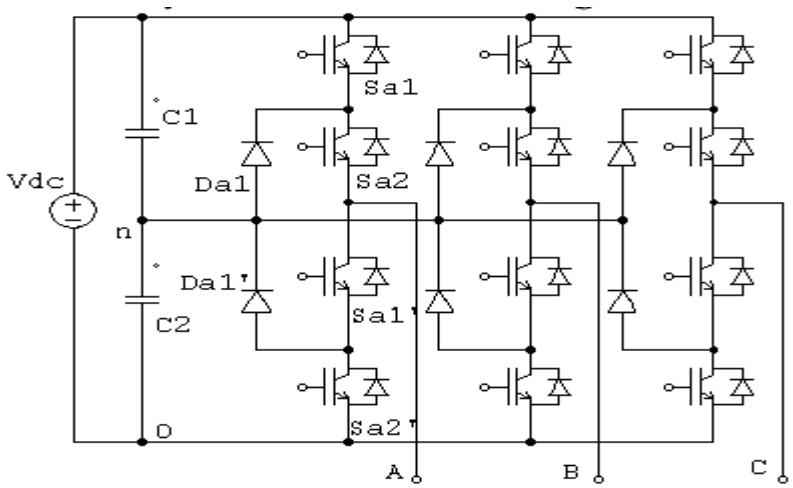

Figure.1. Structure of 3-phase, 3-Level Diode clamped Inverter.

The switching states of the inverter are shown in Table I for one leg. It gives the output pole voltage V_{AO}, output line voltage V_{AB} and switch state. Switch state '1' means 'on' and '0' means 'off'[7-10]. This switching pattern can be achieved by means of different multilevel control strategies such as square wave switching, sine-triangle comparison method (SPWM), space vector modulation (SVM), selective harmonic elimination technique, hysteresis current control, sigma-delta modulation etc. Of these methods, sinusoidal pulse width modulation (SPWM) is the simple and cost effective method to implement.

NEUTRAL POINT POTENTIAL VARIATION AND ITS ANALYSIS

Neutral point voltage variation is the inherent issue in diode clamped inverter. The main reason is that there is the necessary split point in the capacity bank of the DC bus[11-12]. This neutral point is a floating point where the potential will change if there is any NP current. Again NP voltage variations need to be mitigated because they may cause start-up failure, CMV and over voltages across the switching devices. The neutral point voltage V_{np} can be expressed as

$$V_{np} = \frac{1}{C_1+C_2}\int I_n\,(t)dt = \frac{1}{2C}\int I_n\,(t)dt \qquad (1)$$

Because the neutral current I_n is the inherent current in the NPC currents, the NPP voltage V_{np} cannot be minimized to zero without some additional compensation currents added to the NP point to cancel the neutral current I_n. Hence to reduce NP voltage variation $V_{np.}$ Two methods can be applied according to above equation one is to reduce the neutral current I_n by inducing or compensation current and second is increase the DC bus capacitance C_1,C_2 if the maximum I_n and the inverters output frequency are determined.

The first method is widely investigated in the inverter topologies and arithmetical methods including PWM modulation and closed loop control of the NP voltage. For the second method, it is fit for the fixed higher output frequency inverters because a reasonable capacitance value can be applied.

Hence,

$$V_{np} = \frac{1}{2C}\int I_n\,(t)dt = \frac{1}{2C}\int I_{n\,fund}\ sin(\omega t + \theta)dt \quad (2)$$

$$V_{np}=\frac{I_n}{6C\omega} \quad (3)$$

where 'ω' is the fundamental frequency

From equation (3) the NP voltage will become very large if the inverter runs at very low output frequency.

In the following analysis, it is assumed that the carrier frequency is enough high as compared with the fundamental output frequency of the NPC-VSI. To produce less output harmonics than those of a conventional PWM inverter having 6 switching devices, switching in one phase should be performed between the positive potential of *+E* and the neutral potential of *N*or between the negative potential of *-E* and the neutral potential of *N* **.** Consequently, the NPC-VSI outputs a desired voltage as an average voltage during a carrier period, which is obtained by switching between *+E* and *N* for a positive voltage or between *N* and *-E* for a negative voltage. The NPC-VSI adopting the above-mentioned switching scheme produces lower harmonics in the output voltage and current than the conventional PWM inverter dose. Furthermore, it is assumed that the output voltages and currents are sinusoidal as follows:

$$V_a = M\sin\phi + V_o$$
$$V_b = M\sin(\phi-120^o) + V_o$$
$$V_c = M\sin(\phi+120^o) + V_o \quad (4)$$
$$i_a=\sqrt{2}\ I\sin(\phi-\theta)$$
$$i_b=\sqrt{2}\ I\sin(\phi-\theta-120^o)$$
$$i_c=\sqrt{2}\ I\sin(\phi-\theta+120^o) \quad (5)$$

Here, three phase voltages and currents, and the angular frequency are expressed by normalizing with respect to the half of the dc link voltage *E*, the rated current I_R, and the rated angular frequency ω_R, respectively. The modulation index is expressed by M, and V_o means the zero sequence output voltage of the NPC-VSI. When any phase is clamped to the neutral point, the neutral current flows so that the neutral potential varies from the centre potential of the dc link. Fig.1 shows the relationship between an average phase voltage and a time ratio of the neutral-point-clamped phase output. At zero phase voltage, the output terminal of the phase is always clamped to the neutral point, so that the time ratio is 1. In proportion as the increase of the absolute value of the phase voltage the time ratio decreases, and it becomes zero at &*E***.** Consequently, the time ratio in each phase is shown by the following equation.

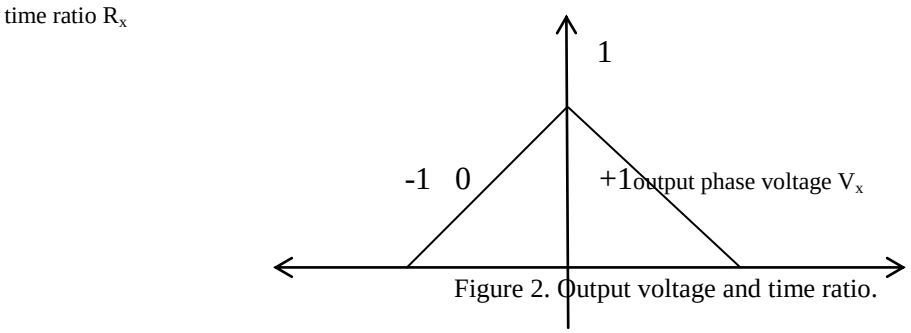

Figure 2. Output voltage and time ratio.

$$R_x = 1 \quad (V_x = 0) \quad \begin{cases} 1\text{-}V_x & (V_x>0) \\ (x=a,b,c) & (6) \\ 1+V_x & (V_x< 0) \end{cases}$$

Since a phase current ***i,*** flows out of the neutral point through its corresponding clamp-diode, the average neutral current in the phase is the product of the phase current*i*, and the time ratio R,. Therefore, the average neutral current during a modulation period is given by

$$i_n= R_a\, i_a + R_b\, i_b + R_c\, i_c \qquad (7)$$

and the normalized neutral potential variation with respect to the centre potential of dc link is easily calculated by the following equation.

$$V_n=-\frac{I_R}{2CE}\int i_n\, dt \qquad (8)$$

The analysis should be performed in six sections shown in Fig.4, because the polarity of the phase voltage alters R, (x=a,b,c). In section [I], i.e., in the case that the u-phase voltage is positive and the v- and w-phase voltages are negative, the average neutral current is derived from substitution of above equations.

$$i_n=M\sqrt{2}\, I\left\{\frac{1}{2}cos\theta + \cos(2\varphi-\theta)\right\} - 2Vo\sqrt{2}\, I\sin(\varphi\text{-}\theta) \qquad (9)$$

the normalized neutral point potential V_n,is calculated by

$$V_n=A.\overline{V_n} \qquad (10)$$

$$\overline{V_n}= -\frac{\boldsymbol{I}}{\boldsymbol{\omega}}\left\{\frac{\boldsymbol{M}}{\boldsymbol{2}}\{\varphi cos\theta + sin(2\varphi-\theta)\} + 2Vocos(\varphi-\theta)\right\} + \boldsymbol{Vno} \qquad (11)$$

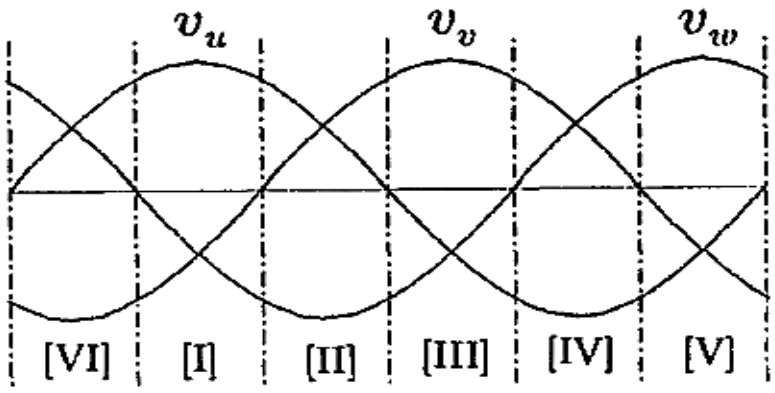

Figure 3. Division of analysis period.

where, $$A = -\frac{\sqrt{2}I_R}{2\omega RCE} \quad (12)$$

$\overline{V_n}$ means a generalised neutral point irrespectively of the ratings of the NPC-VSI, and V_{no} is its initial value. The idea of the generalised NPP can simplify a design of the NPC-VSI. If the generalised NPP is analysed for a NPC-VSI system, the analysis and design results are applicable to other systems having different ratings.

The neutral current in section [II] is obtained by the similar way to the calculation of (9).

$$i_n = M\sqrt{2}\, I\left\{\frac{1}{2}cos\theta + \cos(2(\varphi + \frac{2\pi}{3}) - \theta)\right\} - 2Vo\sqrt{2}\, I \sin(\varphi + 120^o - \theta) \quad (13)$$

The following equation shifts the angle of φ by $\frac{\pi}{3}$

$$\varphi = \varphi' + \frac{\pi}{3} \quad (14)$$

Therefore, substituting the above equation derives as follows:

$$i_n = -M\sqrt{2}\, I\left\{\frac{1}{2}cos\theta + \cos(2\varphi' - \theta)\right\} - 2Vo\sqrt{2}\, I \sin(\varphi' - \theta) \quad (15)$$

In the sections [III]-[VI], the neutral current is similarly calculated. As a result, quite the same form as that in section [I] or section [II] is obtained in sections [III] and [V] or in sections [IV] and [VI], respectively. In the case of ω_o=O, the neutral point potential varies at three times as high as the output fundamental frequency, because the sign of the neutral current changes every 60'. The dc component of the zero sequence voltage moves away the neutral point potential from the centre potential of the dc link, because of the second term with the same sign in Eqs.(9) and (14).In this case, an excessive high voltage may be applied to the switching devices of the NPC-VSI. To prevent the problem, it is necessary to eliminate any dc component in the zero sequence output voltage.

Neutral Point Current Analysis

The neutral point current can be generated by the unbalanced load. The common mode voltage caused by varying DC bus voltage or the NPC inverter itself. Even if the load is balanced and the NP potential is not varied, there still are NP currents. In the following analysis, it is assumed that there is no NP voltage variation and load is balanced. It is assumed that the normalised output voltage and unnormalised current are sinusoidal as follows

$$V_a = M\sin(\omega t) \quad (16)$$

$$V_b = M\sin(\omega t - 120^o) \quad (17)$$

$$V_c = M\sin(\omega t + 120^o) \quad (18)$$

$$i_a = I\sin(\omega t - \phi) \quad (19)$$

$$i_b = I\sin(\omega t - \phi - 120^o) \quad (20)$$

$$i_c = I\sin(\omega t - \phi + 120^o) \quad (21)$$

Where 'ω' is output frequency. I is output total peak current and ϕ is load angle. The modulation index is expressed as M.The total DC bus voltage is V_{dc}. The NP current can be expressed as follows

$$i_n = i_{na} + i_{nb} + i_{nc} \quad (22)$$

Here i_{na},i_{nb},i_{nc} are the phase a,b,and c neutral currents respectively.

When any phase output is clamped to the neutral point, the NP current related to that clamped phase goes into or out of the neutral point.

The main disadvantage is the neutral point voltage variation problem. It is an inherent problem because DC bus capacitor bank consists of two series connected sub capacitor banks as shown in Fig.1. When the three phase load is not completely balanced there will be unequal charging of the DC bus capacitors that induce NP voltage variation. The load unbalance and therefore the NP voltage variation can be significant during the start-up of the NPC inverter driving an AC motor or when the NPC inverter drives the AC motor at a low speed I_n these cases, the lower frequency NP current causes a larger NP voltage variation.

The fluctuations of the NP voltage can cause the switching devices to operate un safely if the unbalance continues to degrade. If that happened during motor start up, the start-up may sometimes fail. If this happens in the low speed operation, it induces more distortion in the output voltage and cause the AC motor to produce torque ripple. Thus the fluctuation of NP voltage is a very important problem that needs to be solved for NPC inverters.

RESULTS AND DISCUSSION

Performance Evaluation of phase disposition carrier based PWM for three level NPC multilevel inverter using small DC link capacitors is simulated using MATLAB. Simulink model shown in Fig. 4 which consists of three phase full wave rectifier, three level NPC inverter and carrier based PWM signals.

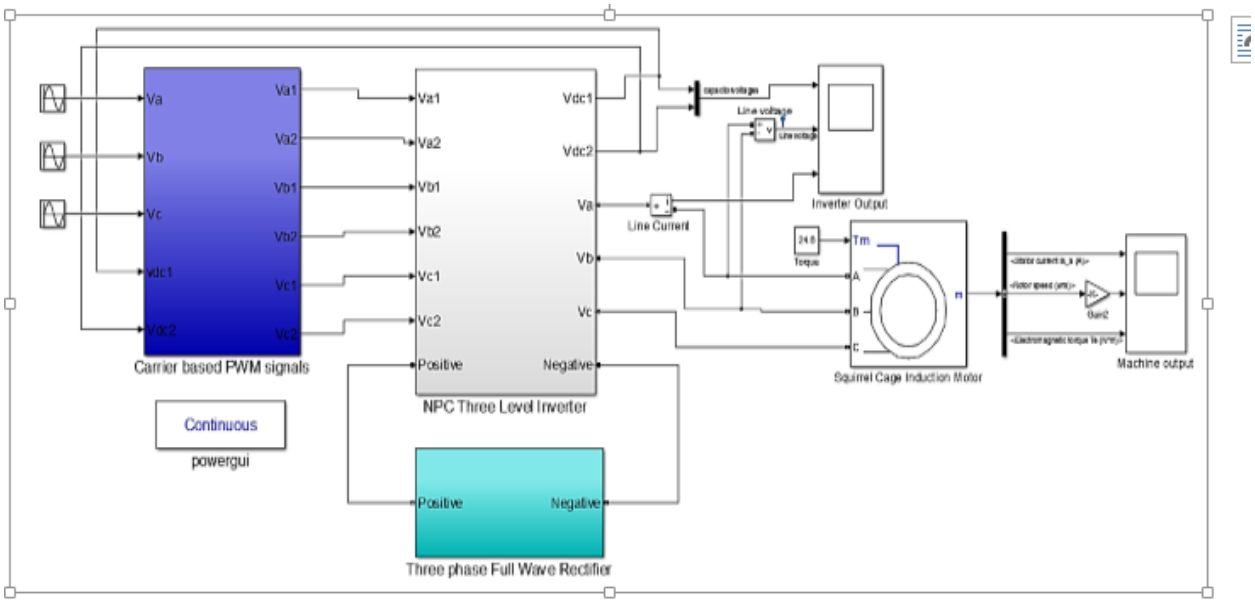

Figure 4. Simulink block of carrier based PWM forthree level neutral clamped inverter using small DC link capacitors.

A. Waveforms using C=3.3mF

The simulation results of three level diode clamped inverter using phase disposition technique using parameters c=3.3mF capacitor, $\omega c = 2\pi \cdot 1000$ rad/s, modulation index (m_a) = 1.1547 at rated load are shown from Fig.5 to Fig.8

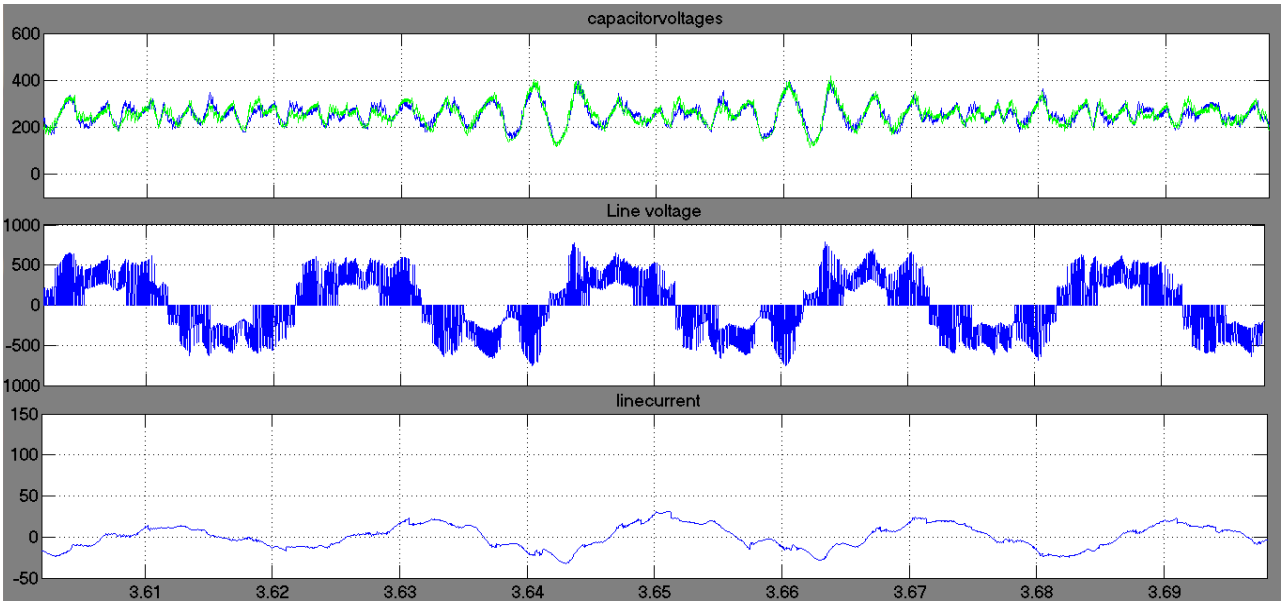

Figure 5. Capacitor voltages, line voltage (V_{AB}) and current (i_A).

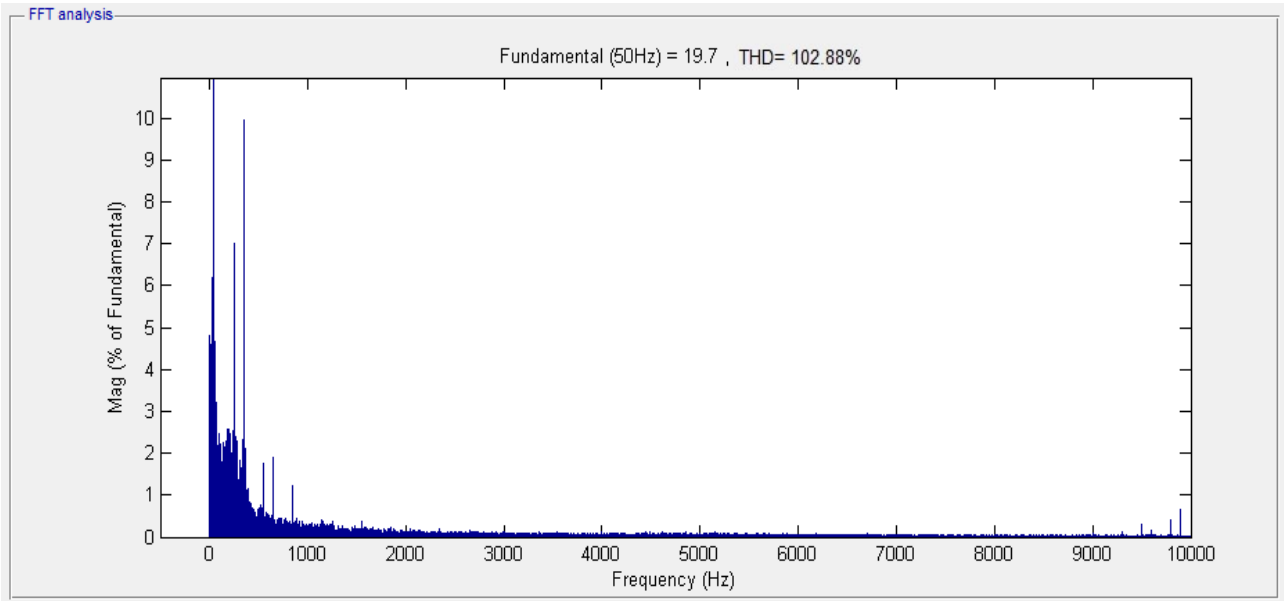

Figure 6. THD of line current.

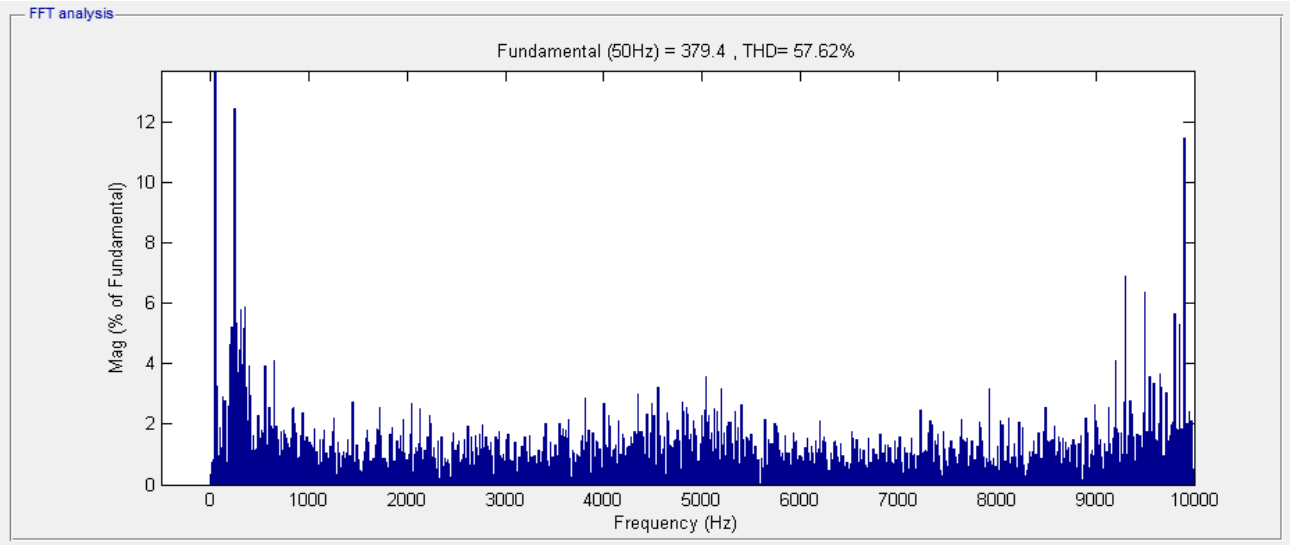

Figure 7. THD of line voltage.

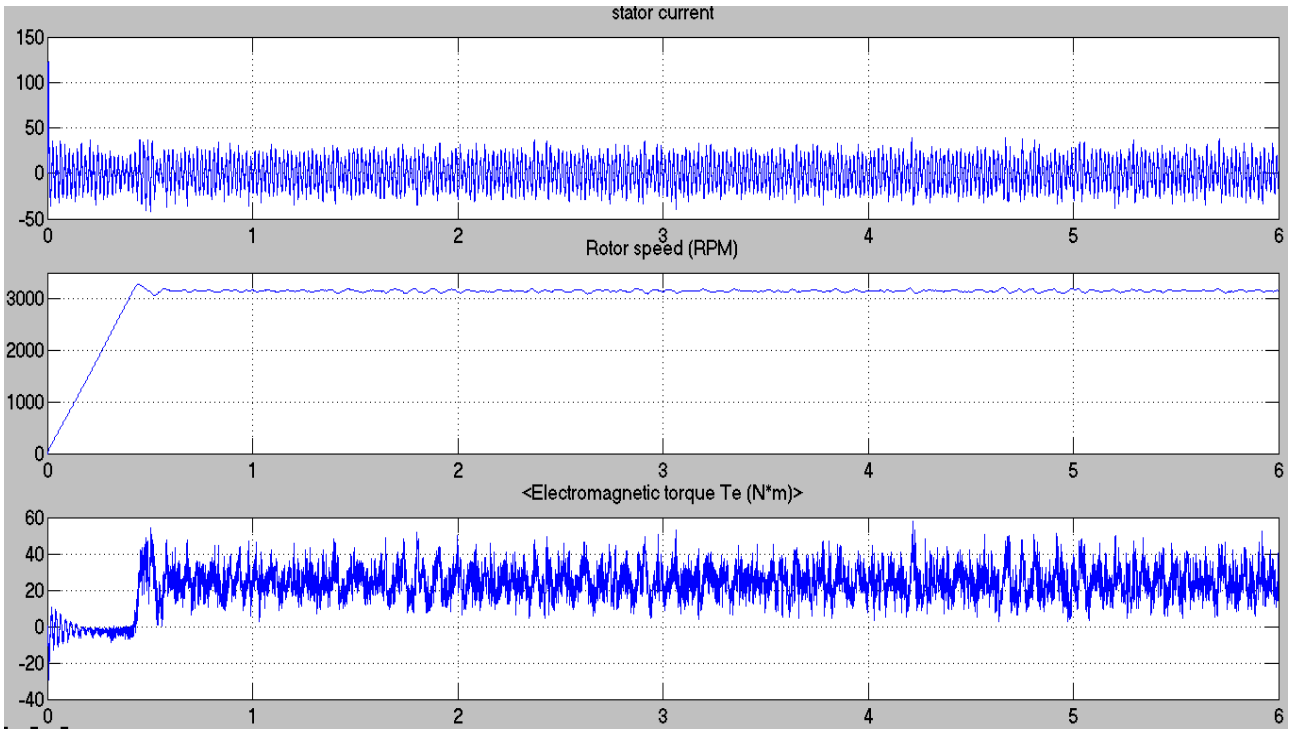

Figure 8. Line current, speed and electromagnetic torque.

B. Waveforms using C=14μF

Fig.9 to Fig.16 presents the resultsof three level diode clamped inverter using phase disposition technique using parameters c=14μF capacitor, $\omega c = 2\pi \cdot 1000$ rad/s, modulation index (m_a) = 1.1547 at rated load.

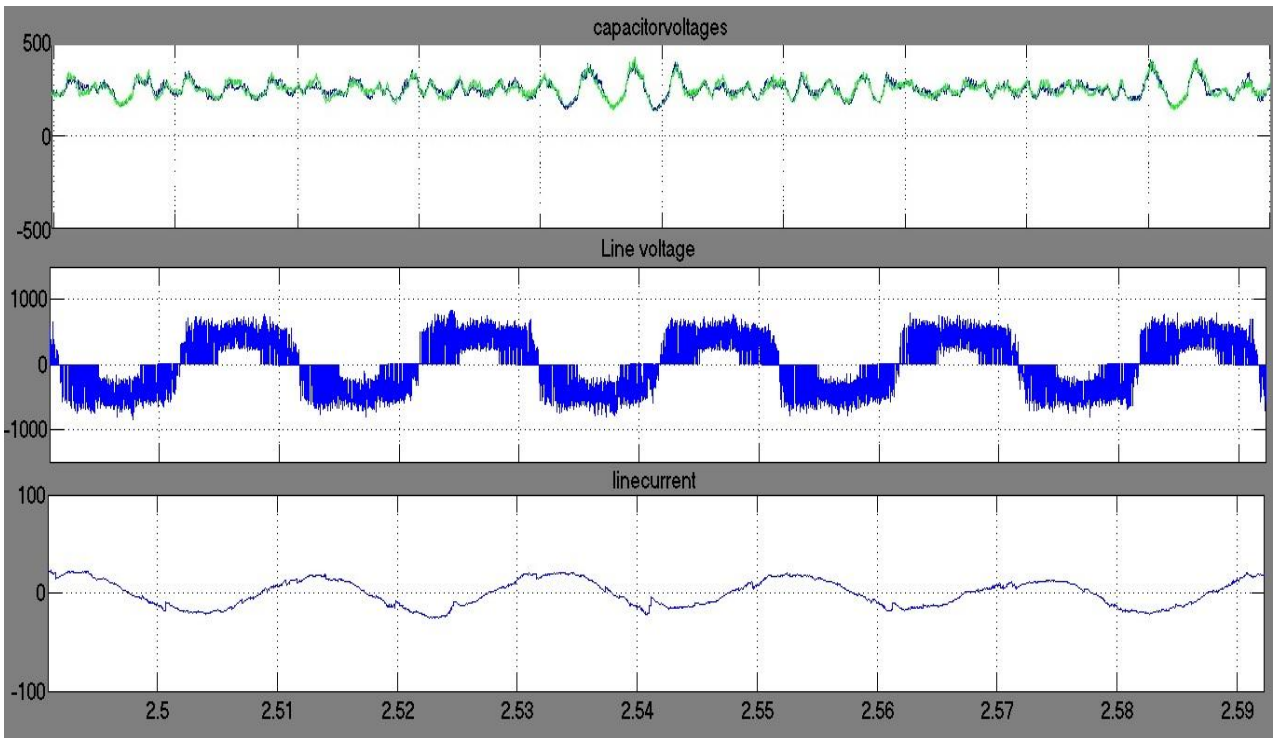

Figure 9. Capacitor voltages, line voltage (V_{AB}) and current (i_A).

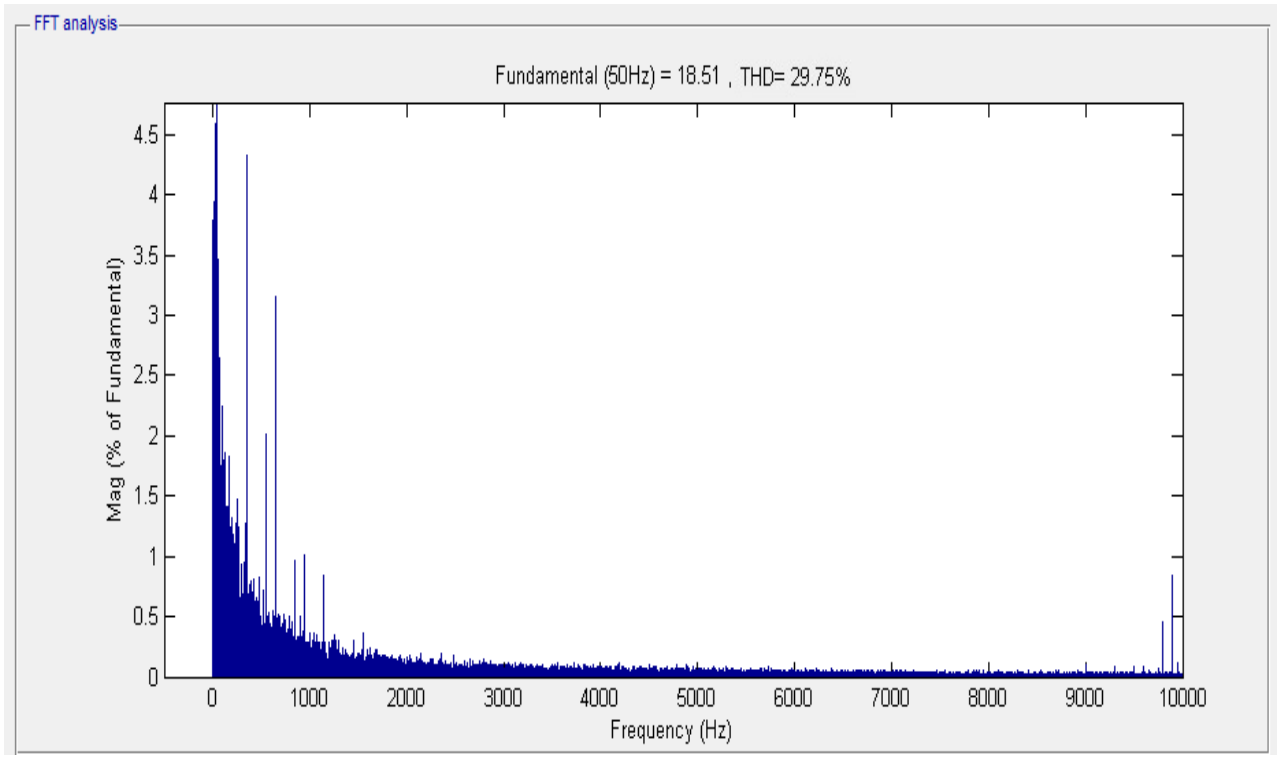

Figure 10. THD of line current.

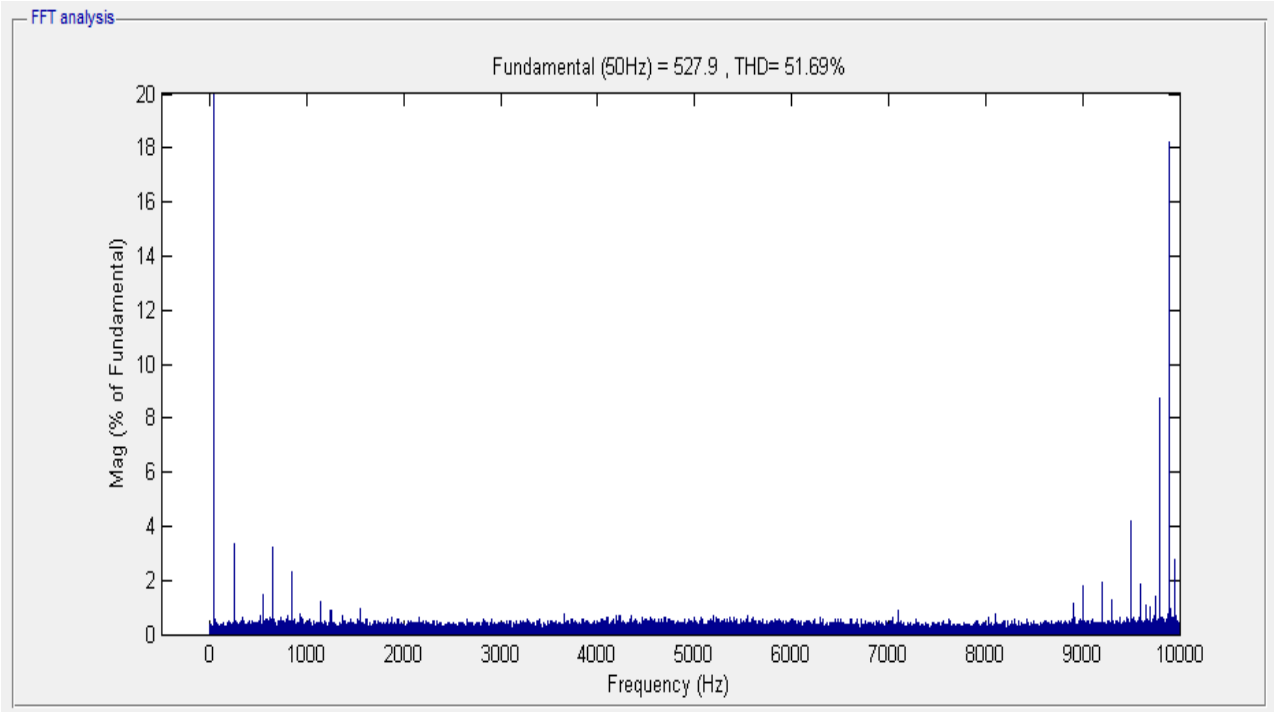

Figure 11. THD of line voltage.

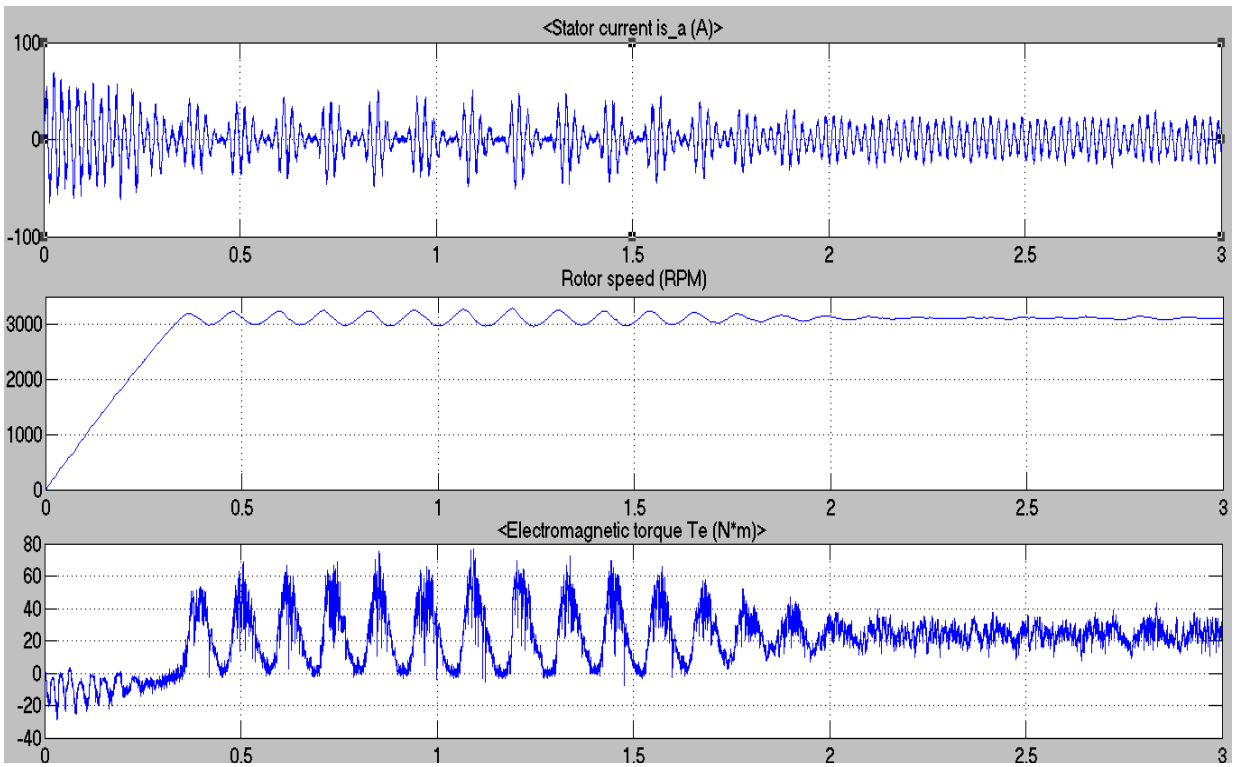

Figure 12. Line current, speed, electromagnetic torque.

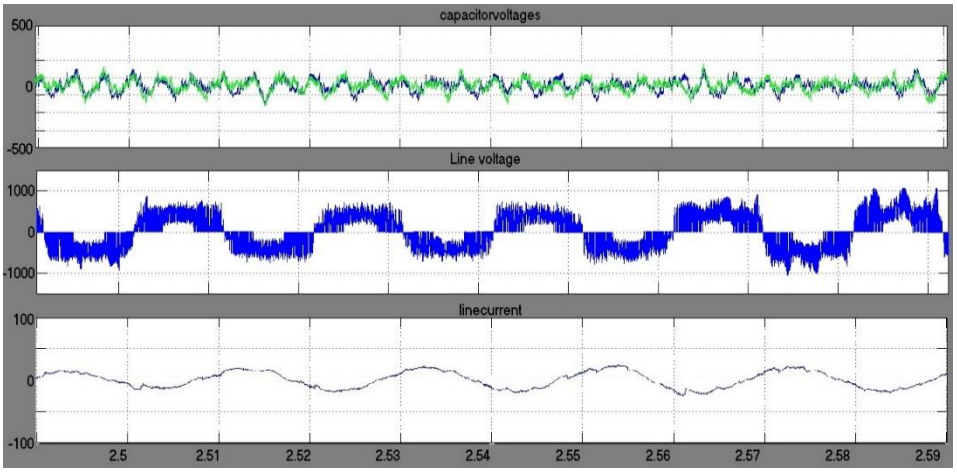

Figure 13. Capacitor voltages, line voltage (V_{AB}) and phase current (i_A)

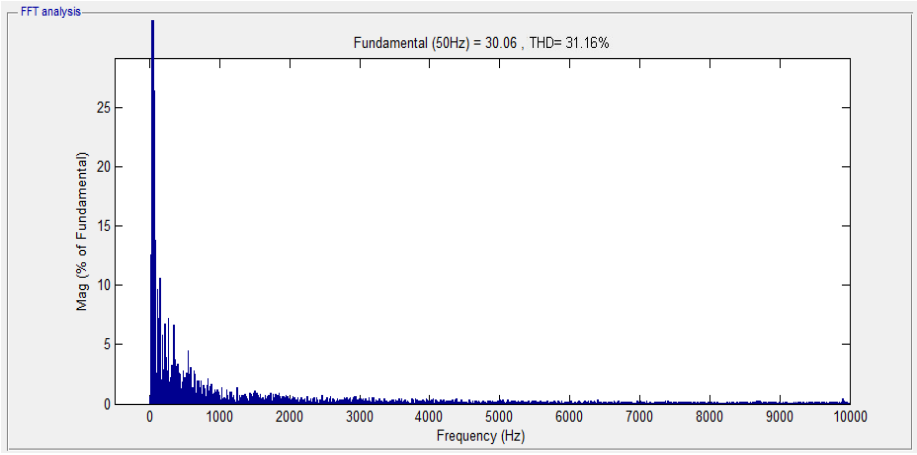

Figure 14. THD of line current.

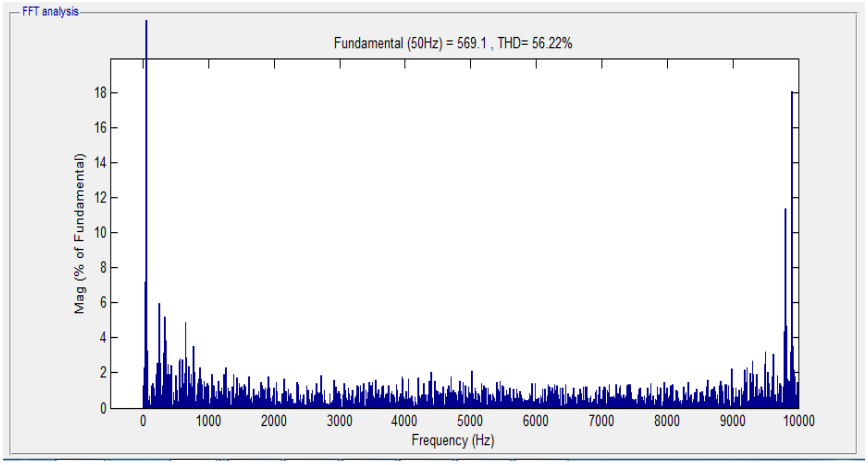

Figure 15. THD of line voltage.

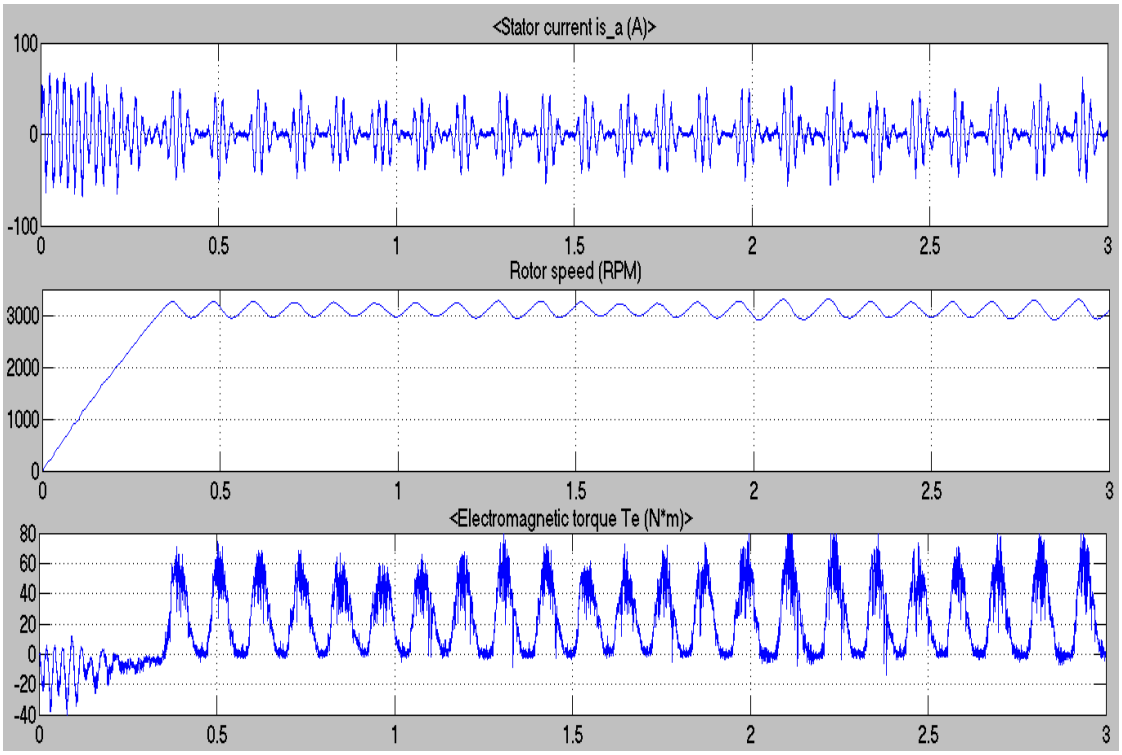

Figure 16. Line current, speed and electromagnetic torque.

The FFT analysis is carried out for voltage and current and the THD is tabulated in tables I to III.

Table I. Voltage and Current THD at K_p=-0.0014

	ω_c *(rad/s)*	C_{dc}	*Voltage(%)*	*Current(%)*
			PD	***PD***
Full load	$2\pi \cdot 1000$	3.3milli farad	57.62	102.88
		14micro farad	51.69	29.75
	$2\pi \cdot 500$	14micro farad	56.22	31.16
Half load	$2\pi \cdot 1000$	3.3milli farad	58.87	49.67
		14micro farad	52.69	59.37
	$2\pi \cdot 500$	14micro farad	53.11	21.62
No load	$2\pi \cdot 1000$	3.3milli farad	56.04	35.29
		14micro farad	56.32	27.76
	$2\pi \cdot 500$	14micro farad	54.41	50.79

Table II. Voltage and current THD (%) using PD technique at various modulation indices (C_{dc}=14μF, K_p=-0.0014 at Full load=24.6 N-m)

Modulation index	*Voltage (%)*	*Current (%)*
1.1547	51.69	29.75
1	49.63	17.80
0.9	52.35	22.10
0.8	51.16	19.60
0.75	50.91	19.16
0.7	80.07	17.96
0.65	49.94	17.44

Table III. Voltage and current THD (%) with different C_{dc} .(K_p=-0.0014,Full load of 24.6Nm)

C_{dc}	*Voltage(%)*	*Current(%)*
3.3 milli farad	57.62	102.88
2.2 milli farad	48.60	80.71
1.1 milli farad	49.09	73.60
0.55 milli farad	49.37	68.71
0.11 milli farad	44.31	44.25
55 micro farad	47.16	36.72
14 micro farad	51.69	29.75
7 micro farad	52.71	30.84

CONCLUSION

An NPC three-level inverter with small dc-link capacitors is presented in this paper. The inverter utilizes a modulation strategy with zero average neutral-point current in a switching period. The modified reference signals are used for carrier-based phase disposition modulation strategy. The controller does not require the information of the output phase current. The controller performance is verified for induction machine-based drive with 3.3mF and 14μF dc-link capacitors. The simulation results show the operation of the drive at maximum modulation index of 1.1547. The simulation results show that the controller is able to maintain balanced capacitor voltages with 10-kHz switching frequency in the presence of 300-Hz ripple of the dc-link voltages caused by a six-pulse rectifier. It is also shown that the small dc-link capacitor-based inverter improves the line current THD, but the implemented modulation strategy causes low-order harmonics in the machine current since average dc-link voltage is used for duty cycle calculation. The performance for dc-link unbalance condition is also simulated for different gains of the PI controller. A fast settling time is achieved with the higher absolute gain.

ACKNOWLEDGMENT

We thank the Science and Engineering Research Board (SERB), Government of India, New Delhi for providing Research Project under 'Fast Track Scheme for Young Scientists' to carry out the Research on Multilevel Inverters. We also thank Principal and Head, Department of Electrical Engineering, University College of Engineering (Autonomous), Osmania University, Hyderabad.

REFERENCES

[1] J. S. Lai and F. Z. Peng, "Multilevel converters – a new breed of power converters," IEEE Trans. Industry Applications, vol. 32, pp. 509–517, May/June 1996.

[2] A.Nabae, I. Takahashi, and H. Akagi, "A new neutral-point clamped PWM inverter," IEEE Trans. Industry Applications, vol. IA-17,pp. 518–523, September/October 1981.

[3] G. Carrara, S. Gardella, M. Marchesoni, R. Salutari, and G. Sciutto, "A new multilevel PWM method: a theoretical analysis," IEEE Trans.Power Electronics, vol. 7, no. 3, pp. 497–505, July 1992.

[4] N.Susheela, P.Satish Kumar, B.Sirisha, "Hybrid Topologies of Multilevel Converter for Current Waveform Improvement", International Journal of Inventive Engineering and Sciences (IJIES), ISSN: 2319–9598, Volume-1, Issue-4, pp.29-37, March, 2013.

[5] S. Ogasawara and H. Akagi, "Analysis of variation of neutral point potential in neutral point clamped voltage source PWM inverters," in Conf. Rec. IEEE IAS Annu. Meeting, 1993, pp. 965–970.

[6] Ramkrishan Maheshwari, Stig Munk-Nielsen,and Sergio Busquets-Monge, "Design of Neutral-Point Voltage Controllerof a Three-Level NPC Inverter WithSmall DC-Link Capacitors" IEEEtransactions on industrial electronics, vol. 60, NO. 5, MAY 2013

[7] F. Z. Peng, J. S. Lai, J.W.McKeever, and J. VanCoevering, "A multilevel voltage-source inverter with separate DC sources for static var generation," IEEE Trans. Industry Applications, vol. 32, no. 5, pp. 1130–1138,September 1996.

[8] L. M. Tolbert and T. G. Habetler, "Novel multilevel inverter carrier based PWM method," IEEE Trans. Industry Applications, vol. 25, no. 5, pp. 1098–1107, September/October 1999.

[9] J. Rodriguez, J. S. Lai, and F. Z. Peng, "Multilevel inverters: survey of topologies, controls, and applications," IEEE Trans. Industry Applications, vol. 49, no. 4, pp. 724–738, August 2002.

[10] L. M. Tolbert, F. Z. Peng, and T. Habetler, "Multilevel converters for large electric drives," IEEE Trans. Industry Applications, vol. 35,pp. 36–44, January/February 1999.

[11] N.Susheela, P.Satish Kumar and C.H.Reddy, "Performance Analysis of Four Level NPC and NNPC Inverters using Capacitor Voltage Balancing Method" IEEE Uttar Pradesh Section International Conference on Electrical, Computer and Electronics Engineering (UPCON), pp. 212-217, Dec 2016.

[12] F. Z. Peng, "A generalized multilevel converter topology with self-voltage balancing," IEEE Trans. Industry Applications, vol. 37,IEEE Industry Applications Society Annual Meeting, pp. 611–618,March/April 2001.